one of said side walls and a third portion formed over at least a first portion of said top surface of said floating gate and being separated from said floating gate by said second insulation layer, said second portion having a surface substantially parallel to and opposing said first side wall;

an erase gate formed over a second one of said side walls and over at least a second portion of said top surface of said floating gate and being separated from said second one of said side walls and said portion of said top surface of said floating gate by said second insulation layer;

a drain region formed in a portion of said substrate proximate said control gate; and

a source region formed in a portion of said substrate proximate said erase gate;

whereby during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential applied to the erase gate, stored electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim tunneling process.

9. (Amended) A memory array disposed on a substrate as recited in claim 8 wherein said floating gate has at least a substantial portion thereof disposed over said channel region and is separated therefrom by said first insulating layer, said control gate is substantially placed on one side of said floating gate and separated therefrom by said second insulation layer, said erase gate is substantially placed on a second side of said floating gate and is separated therefrom by said second insulation layer, said drain region is substantially disposed on said one side of said floating gate, and said source region is substantially disposed on said second side of said floating gate.

16. (Amended) A semiconductor device having at least one transistor, the device comprising:

a substrate having a channel region;

a first insulating layer disposed over said channel region and over at least a portion of said substrate;

a floating gate having at least a substantial portion thereof disposed over disposed over said channel region and separated therefrom by said first insulating layer, said floating gate having at least two side walls and a top surface;

a second insulating layer disposed over said side walls and over said top surface of said floating gate;

a control gate having a first portion disposed over a first portion of said channel region and being separated therefrom by said second insulating layer, a second portion formed over a first one of said side walls and a third portion formed over at least a portion of said top surface of said floating gate and being separated from said floating gate by said second insulation layer, said second portion having a surface substantially parallel to and opposing said first one of said side walls;

an erase gate formed over a second one of said side walls and over at least a second portion of said top surface of said floating gate and being separated from said second one of said side walls and said portion of said top surface of said floating gate by said second insulation layer;

a source region formed in a portion of said substrate proximate said erase gate; and a drain region formed in a portion of said substrate proximate said control gate;

whereby during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential applied to the erase gate, stored electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim tunneling process.